What is claimed is:

1. A semiconductor memory device comprising:

a plurality of memory cells, each of which is assigned a unique address to be accessed by a corresponding address;

a plurality of redundant cells being replaceable with the memory cells;

a redundancy repair control circuit replacing a plurality of predetermined memory cells among the memory cells with the redundant cells; and

a test mode control circuit invalidating an operation of the redundancy repair control circuit and assigning an additional unique address to the redundant cells so that all of the memory cells and the redundant cells are accessible during a test mode.

2. A semiconductor memory device according to claim 1, wherein the test mode control circuit disabling an output of the redundancy repair control circuit.

3. A semiconductor memory device according to claim 1, further comprising a sense amplifier and an input/output circuit.

4. A semiconductor memory device according to claim 1, further comprising a row decoder and a redundant row decoder.

5. A semiconductor memory device according to claim 1, wherein the test mode control circuit includes a plurality of gate circuits.

6. A semiconductor memory device comprising:

a memory cell array including a plurality of memory rows assigned addresses designated from 1 to n including non-redundant addresses and redundant addresses, wherein n is a natural number, and a plurality of redundant memory rows;

a row decoder accessing the memory rows in response to the non-redundant addresses;

a redundant row decoder accessing the redundant memory rows in response to the redundant addresses;

a redundant address determining circuit coupled to the redundant row decoder for determining the redundant addresses among the addresses; and

a test mode control circuit invalidating an operation of the redundant address determining circuit and assigning an additional address assigned n+1 to m to the redundant rows so that all of the memory rows and the redundant rows are accessible during a test mode, wherein m is a natural number grater than n.

7. A semiconductor memory device according to claim 5, wherein the test mode control circuit disabling an output of the redundant address determining circuit.

8. A semiconductor memory device according to claim 5, further comprising a sense amplifier and an input/output circuit.

9. A semiconductor memory device according to claim 6,

wherein the test mode control circuit includes a plurality of gate circuits.

10. A semiconductor memory device according to claim 6, further comprising an additional memory cell array including a plurality of memory rows, wherein the redundant memory rows are used for the memory cell array and the additional memory cell array.

11. A semiconductor memory device according to claim 6, further comprising an address buffer.

12. A semiconductor memory device comprising:

a memory cell array including a plurality of memory rows assigned addresses designated from 1 to n, the addresses including non-redundant addresses and redundant addresses, wherein n is a natural number;

a plurality of redundant memory rows;

a row decoder coupled to the memory cell array for accessing the memory rows in response to the non-redundant addresses;

a redundant address determining circuit determining the redundant addresses among the addresses;

a redundant row decoder coupled to the redundant memory rows and the redundant address determining circuit for accessing the redundant memory rows in response to the redundant addresses; and

a test mode control circuit invalidating the redundant

address determining circuit and assigning an additional address assigned n+1 to m to the redundant rows so that all of the memory rows and the redundant memory rows are accessible during a test mode, wherein m is a natural number grater than n.

13. A semiconductor memory device according to claim 12, wherein the test mode control circuit disabling an output of the redundant address determining circuit.

14. A semiconductor memory device according to claim 12, further comprising a sense amplifier and an input/output circuit.

15. A semiconductor memory device according to claim 12, wherein the test mode control circuit includes a plurality of gate circuits.

16. A semiconductor memory device according to claim 12, further comprising an additional memory cell array including a plurality of memory rows, wherein the redundant memory rows are used for the memory cell array and the additional memory cell array.

17. A semiconductor memory device according to claim 12, further comprising an address buffer.